ABSTRACT

A Pulse Clock Delay (PCT) apparatus (208) includes a selectable plurality (Nd) of series-connected pulse transition delay units (209) from a total plurality (Nmax) of such units. Each unit provides an incremental proximal node (n1a) and an adjacent electrically isolated second intermediate node (n1b) where the first and second intermediate nodes are in a shorter (215a, 215b) of two signal paths having respective proximal and spaced apart distal ends (212, 216) in an electrical network. Control means (205), responsive to the difference in electrical length between the two signal paths (214, 215), configures the switchable selection means to select a particular number of delay segments such that the propagation of a first edge transition (102) through the series combination of the shorter first path (215a, 215b) and the delay segment (208) is delayed sufficiently to arrive at the second path distal end (216) within +/- DELTA t of the time of arrival of the first edge transition propagating through the second path. Multiple PCDs may be distributed on a PCB to compensate delay differences for multiple pairs of unequal length bifurcated clock/signal lines.